OVERLAP STACKING OF CENTER BUS BONDED MEMORY CHIPS FOR DOUBLE DENSITY AND METHOD OF MANUFACTURING THE SAME

ABSTRACT OF THE DISCLOSURE

An approach to DRAM memory chip packaging leveraging the chip center position for wire bond pads to minimize time-of-flight and impedance effects resulting from stacking in a BGA application. A top layer of a dual device stack of center bus chips is stacked with an offset in a single direction with respect to a bottom layer of the dual device stack. The top layer of chips may be wire bonded to the opposite side of the module substrate. The center bus may be made to traverse to the substrate between two memory devices on the lower layer. To assemble the offset stacking devices into a high density module, devices are placed sequentially on a module substrate such that approximately one half of the protruding lower memory device is used as a support for the overhanging upper memory device chip of the next device stack.